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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,004	11/07/2001	Takuji Matsumoto	215544US2	4595

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EXAMINER
SEFER, AHMED N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,004	MATSUMOTO ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-20* is/are pending in the application.

4a) Of the above claim(s) *4-7 and 13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 8-12* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *13* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. The amendment filed on 2/3/03 has been entered and claim 2 has been cancelled.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1 and 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsumoto et al. US Patent No. 6,455,894.

Matsumoto et al disclose in figs. 1-13 a semiconductor device having an SOI structure including a semiconductor substrate 1, a buried insulating layer 2 and an SOI layer 3, comprising: a MOS transistor provided in an element formation region of said SOI layer; and a partial isolation region provided in said SOI layer and serving to isolate said element formation region, said partial isolation region including a partial insulating film 5b provided in an upper layer portion of said SOI layer and a partial insulating film lower semiconductor region 3b to be a part of said SOI layer present in a lower layer portion of said SOI layer, said MOS transistor including: source and drain regions 6 of a first conductivity type selectively formed in said SOI

layer, respectively, wherein said source and drain regions having such depths as to reach said buried insulating layer (as in claim 9); a gate electrode 7 having a gate electrode main part formed through a gate oxide film 4 on a region of said SOI layer between said source and drain regions; and a body region having a body region main part 3a to be a region of a second conductivity type of said SOI layer between said source and drain regions and a body region potential setting portion 3d electrically connected from said body region main part in said element formation region and capable of externally fixing an electric potential, wherein said body region potential setting section includes a body region source/drain adjacent portion in a gate width direction adjacently to said source and drain regions and extended in a gate length direction from said body region main part, said gate electrode further includes a gate extension region extended in said gate length direction from an end of said gate electrode main part and formed on a part of said body region source/drain adjacent portion, and serving to electrically block said body region source/drain adjacent portion and said source and drain regions through said gate extension region, and a thickness of said partial insulating film lower semiconductor region is thinner than thickness of said source and drain regions.

As to claim 8, Matsumoto et al disclose a partial isolation film lower semiconductor region having a second conductivity type formed in contact with said body region, said semiconductor device further comprising an element formation region outside body region of a first conductivity type provided outside said element formation region of said SOI layer and being capable of externally fixing an electric potential, said element formation region outside body region being formed in contact with said partial insulating film lower semiconductor region.

As to claim 10, Matsumoto et al disclose source and drain regions having such depths that a depletion layer extended from said source and drain regions does not reach said buried insulating layer during a normal operation.

As to claim 11, Matsumoto et al disclose in figs. 36-38 source and drain regions having such depths that said buried insulating layer is not reached and a depletion layer extended from said drain region reaches said buried insulating layer during a normal operation.

4. Claims 1 and 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Kunikiyo. US Patent No. 6,545,318.

Kunikiyo discloses in figs. 1-3 a semiconductor device having an SOI structure including a semiconductor substrate 1, a buried insulating layer 2 and an SOI layer 3, comprising: a MOS transistor provided in an element formation region of said SOI layer; and a partial isolation region provided in said SOI layer and serving to isolate said element formation region, said partial isolation region including a partial insulating film 4 provided in an upper layer portion of said SOI layer and a partial insulating film lower semiconductor region 11 to be a part of said SOI layer present in a lower layer portion of said SOI layer, said MOS transistor including: source and drain regions 7/71 of a first conductivity type selectively formed in said SOI layer, respectively, wherein said source and drain regions having such depths as to reach said buried insulating layer (as in claim 9); a gate electrode 6 having a gate electrode main part formed through a gate oxide film 5 on a region of said SOI layer between said source and drain regions; and a body region having a body region main part 10 to be a region of a second conductivity type of said SOI layer between said source and drain regions and a body region potential setting portion 111 electrically connected from said body region main part in said element formation

region and capable of externally fixing an electric potential, wherein said body region potential setting section includes a body region source/drain adjacent portion in a gate width direction adjacently to said source and drain regions and extended in a gate length direction from said body region main part, said gate electrode further includes a gate extension region extended in said gate length direction from an end of said gate electrode main part and formed on a part of said body region source/drain adjacent portion, and serving to electrically block said body region source/drain adjacent portion and said source and drain regions through said gate extension region, and a thickness of said partial insulating film lower semiconductor region is thinner than thickness of said source and drain regions.

As to claim 8, Kunikiyo discloses a partial isolation film lower semiconductor region having a second conductivity type formed in contact with said body region, said semiconductor device further comprising an element formation region outside body region of a first conductivity type provided outside said element formation region of said SOI layer and being capable of externally fixing an electric potential, said element formation region outside body region being formed in contact with said partial insulating film lower semiconductor region.

As to claim 10, Kunikiyo discloses source and drain regions having such depths that a depletion layer extended from said source and drain regions does not reach said buried insulating layer during a normal operation.

As to claim 11, Kunikiyo discloses in fig. 14 source and drain regions having such depths that said buried insulating layer is not reached and a depletion layer extended from said drain region reaches said buried insulating layer during a normal operation.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo in view of Aoki et al. (JP 1-268063).

Kunikiyo discloses the device structure as recited in the claim, but does not teach a drain region having a greater depth than a source region.

Aoki et al disclose in figs 1 and 3 a drain region having a greater depth than a source region.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Aoki et al with the device of Kunikiyo, since that would eliminate the instability of operation due to fluctuatation of a potential in an SOI device as taught by Aoki et al.

Allowable Subject Matter

7. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. US PG-Pub 2002/0105031 disclose an SOI device for eliminating floating body effects.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601.

ANS
April 20, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800